

REMARKS/ARGUMENTS

Favorable reconsideration of this application in light of the following discussion is respectfully requested.

Claims 1-3, 12, 17, 18, 20, 24-27, 36, 41-43 are pending in the present application. Claims 1, 17, 24 and 41 are amended by the present amendment and Claims 4-11, 13-16, 19, 21-23, 28-35, 37-40 and 44-63 are previously withdrawn. Support for amendments to the claims can be found in the disclosure as originally filed, at least in Figures 8 and 12 and corresponding disclosure. Thus, no new matter is added.

In the outstanding Office Action, Claims 1, 2, 17, 18, 24, 25, 41 and 42 were rejected under 35 U.S.C. §102(b) as unpatentable over Allen (U.S. Pat. No. 5,796,511); Claims 3, 26, 27 and 43 were rejected under 35 U.S.C. §103(a) as unpatentable over Allen in view of Morimoto (U.S. Pat. No. 6,169,562); and Claims 12, 20 and 36 were rejected under 35 U.S.C. §103(a) as unpatentable over Allen in view of Suzuki (U.S. Pat. Pub. No. 2003/0156184).

Addressing now the rejection of Claims 1, 2, 17, 18, 24, 25, 41 and 42 under 35 U.S.C. §102(b) as anticipated by Allen, that rejection is respectfully traversed.

Amended Claim 1 recites, in part,

a pixel clock generating unit that generates first and second pixel clocks, which are used for controlling timings of projection of said laser beams, separately for each of said laser light sources, and for performing a phase change of each of said first and second pixel clocks; and

a phase control unit that controls said first and second pixel clocks such that a respective rising period of said first and second pixels clocks is set shorter or longer than a normal clock period a predetermined interval after detection of a respective synchronization detection signal, said phase control unit controlling said first pixel clock independent of said second pixel clock and controlling said second pixel clock independent of said first pixel clock.

Claims 17, 24 and 41 recite similar features regarding control of the implementation of phase change in each of the first and second pixel clocks.

Allen describes a multi-beam scanning system for scanning a curved imaging surface. Further, Allen describes that pixel clocks 212A and 212B are connected to clock phase shifters 214A and 214B which are respectively connected to a dual channel AOM 220 (oscillating mirror).

However, Allen does not describe or suggest a phase control unit that controls said first and second pixel clocks such that a respective rising period of said first and second pixels clocks is set shorter or longer than a normal clock period a predetermined interval after detection of a respective synchronization detection signal.

The outstanding Action cites, on page 2, the AOM 220 of Allen as corresponding to the phase control unit recited in Claim 1. Applicants respectfully traverse this assertion. Specifically, the dual channel AOM 220 of Allen does not control the first and second pixel clocks such that a respective rising period of said first and second pixels clocks is set shorter or longer than a normal clock period. In fact, the dual channel AOM 220 of Allen does not control the clocks at all. Instead, the AOM 220 of Allen merely receives signals from the AOM drivers 217 and modifies the laser 210 based on these signals.

In addition, the AOM 220 of Allen never describes controlling the clocks after detection of a respective synchronization detection signal or delaying the control a predetermined period as is recited in Claim 1.

In a non-limiting example of the claimed invention, Figure 6 illustrates phase control units 21a and 21b which, after receiving respective synchronization detection signals (xlclr0 and xlcr1), control the first and second pixel clocks (clkw0 and clkw1) such that a respective rising period of said first and second pixels clocks is set shorter or longer than a normal clock period by sending signals xpls0 and xpls1. Moreover, Figure 12 provides a non-limiting example of the predetermined interval prd0/prd1 which is executed after detection of

respective synchronization detection signals (xlclr0 and xlclr1) before the control is enacted via xpls0 and xpls1.

In addition, Applicants note that the clock phase shifters 214A and 214B of Allen also cannot be asserted as being the phase control unit recited in Claim 1 as these elements of Allen do not control the first and second pixel clocks such that a respective rising period of said first and second pixels clocks is set shorter or longer than a normal clock period a predetermined interval after detection of a respective synchronization detection signal.

Accordingly, as Allen does not describe or render obvious the features of the claimed invention, Applicants respectfully submit that Claim 1, and similarly Claims 17, 24 and 41 and claims depending therefrom, patentably distinguish over Allen.

Moreover, none of the further cited Morimoto or Suzuki references cure the above noted deficiencies of Allen with regard to the claimed invention.

Consequently, for the reasons discussed in detail above, no further issues are believed to be outstanding in the present application, and the present application is believed to be in condition for formal allowance. Therefore, a Notice of Allowance is earnestly solicited.

Should the Examiner deem that any further action is necessary to place this application in even better form for allowance, the Examiner is encouraged to contact the undersigned representative at the below listed telephone number.

Respectfully submitted,

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